AzureWave Technologies, Inc.

Module IC (SIP)

SMT Process Suggestion

Version 2.0

Document release	Date	Modification	Initials	Approved
Version 0.1	2007/6/25	Initial version	Chipper Chen	CE Huang
Version 0.2	2007/12/10	Stencil opening and bake rule modified	Steven Yeh	Jack Wong
Version 0.3	2008/4/25	Scope update	Yihshang Kao	Jack Wong
Version 0.4	2009/2/11	Reflow parameter modified	Steven Yeh	Jack Wong
Version 0.5	2012/2/7	1. Revised footprint suggestion 2. Window time modified	Ron Chuang	Steven Yeh
Version 0.6	2012/4/9	Baking condition modified	Ron Chuang	Steven Yeh
Version 0.7	2014/05/15	Revise Reflow condition	Allen Huang	Chihhao Liao
Version 0.8	2014/09/02	Update Tape&Reel Baking Temperature and Times	Allen Huang	Chihhao Liao
Version 0.9	2020/01/07	Revise template	Hank Wu	Allen Huang
Version 2.0	2024/10/15	Revise version	Hank Wu	Ricky Wu

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1. Purpose

To define board level SMT process suggestion when customer used Module IC mounting.

2. Scope

For all AzureWave's Module IC(SIP).

3. Production rule

3.1 Footprint and stencil aperture recommendation

3.1.1 Footprint: Footprint shares the same center with pin pad land, and follows below rule to define the size.

3.1.1.1 Rectangle type:

3.1.1.1.1 Outermost layer: Increase the pin pad size about 10% in length & width.

Footprint length = 1.1 * (pin pad land length)

Footprint width = 1.1 * (pin pad land width)

3.1.1.1.2 Others: the same size with pin pad.

3.1.1.2 Round type:

3.1.1.2.1 Outermost layer: Increase the pin pad size about 10% in diameter.

Footprint diameter = 1.1 * (pin pad land diameter)

3.1.1.2.2 Others: the same size with pin pad.

3.1.2 Stencil aperture suggestion

3.1.2.1 The same size with footprint.

3.2 Reflow soldering profile

Table 4-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 4-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

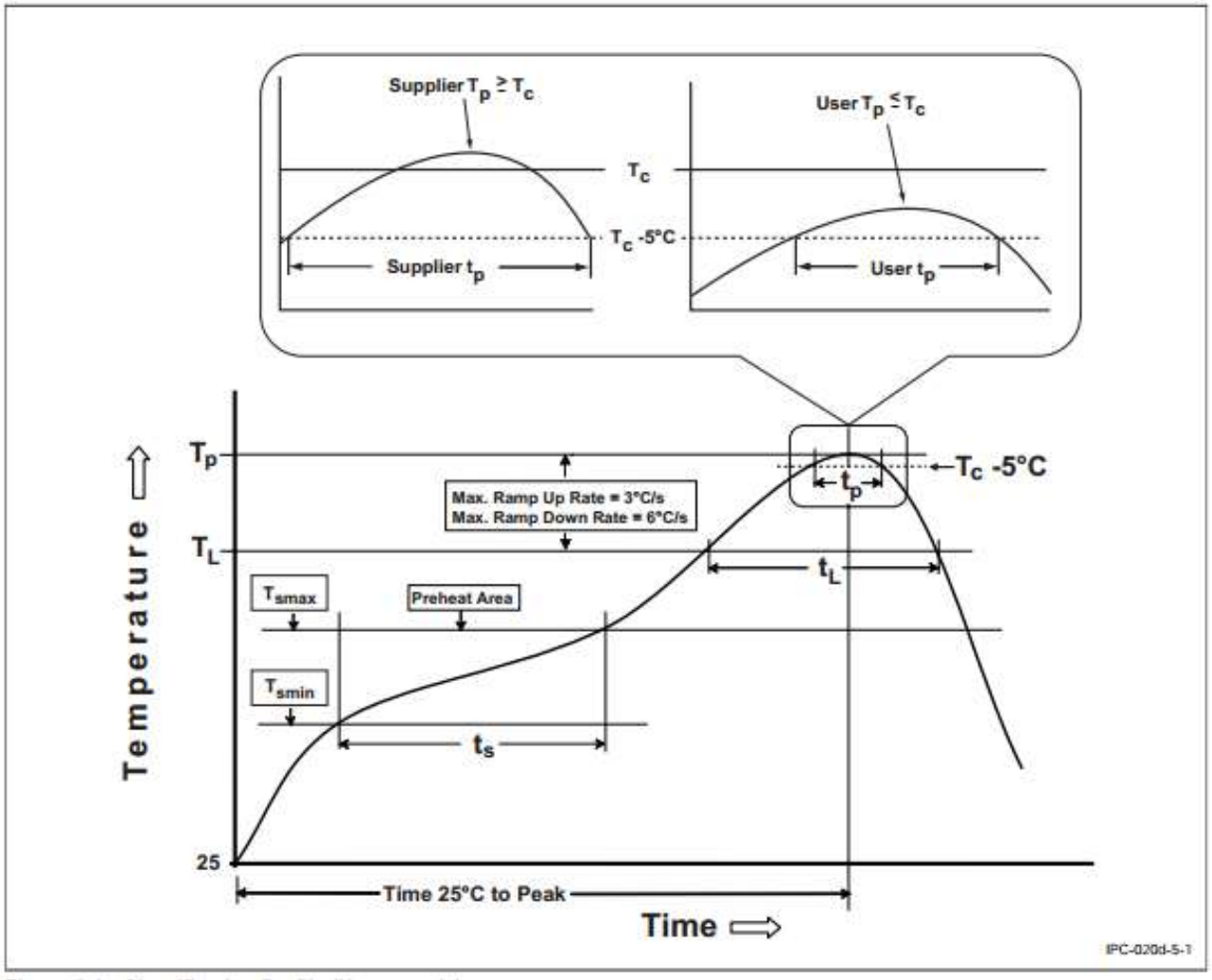

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note: 1. Recommend to supply N_2 for reflow oven

2. N_2 atmosphere during reflow (O_2<300ppm)

4. SIP USE

4.1 Shelf life in Moisture Barrier Bag (MBB): 12 months, at <30℃ and <60% relative humidity (RH)

4.2 Opened MBB: After the dry pack (MBB) has been opened, all module ICs within that bag must complete all solder reflow processing, including rework, prior to the floor life (168 hours), if not, need dry baking to reset the floor life.

4.3 General Consideration for Baking: The oven used for baking shall be vented and capable of maintaining the required temperatures at less than 5% RH.

4.3.1 High Temperature Carriers (Tray): module IC shipped in high temperature carriers can be baked in the carriers at 125℃

4.3.2 Low Temperature Carriers (Tape & Reel): module IC shipped in low temperature carriers may not be baked at any temperature higher than 40℃

4.4 Baking Condition:

4.4.1 High Temperature Carriers

4.4.1.1 Exceeding Floor Life > 72 hours: bake @125℃ 8 hours

4.4.1.2 Exceeding Floor Life ≦ 72 hours: bake @125℃ 6 hours

4.4.2 Low Temperature Carriers

4.4.2.1 Exceeding Floor Life > 72 hours: bake @60℃ ≦5% RH 96 hrs.

4.4.2.2 Exceeding Floor Life ≦ 72 hours: bake @60℃≦5% RH 72 hrs.

4.4.2.3 If a higher bake temperature is required, module IC must be removed from the low temperature carriers to thermally safe carriers, baked, and returned to the low temperature carriers.

4.5 Recommend to baking oven with N2 supplied

4.6 Recommend to reflow oven with N2 supplied

4.7 Baked required with 24 hours at 125+-5℃ before rework process for two modules, one is new module and two is board with module

4.8 Recommend to store at ≦10% RH with vacuum packing

4.9 If SMT process needs twice reflow:

4.9.1 Process flow: (1) Bottom side SMT and reflow → (2) Top side SMT and reflow

4.9.1.1 Case 1: Module IC mounted on Top side. Need to bake when bottom side process over 168 hours window time

4.9.1.2 Case 2: Module IC mounted on bottom side, follow normal bake rule before process

Note: Window time means from last bake end to next reflow start that has 168 hours space.